

1 **What is claimed is:**

1 1. A mask read only memory containing diodes,
2 comprising:

3 a semiconductor substrate;
4 an insulating layer on the semiconductor substrate;
5 a plurality of first conductive lines along a first
6 direction on the insulating layer;
7 a plurality of vertical diodes on the first
8 conductive lines;
9 a plurality of dielectric layers on part of the
10 diodes; and
11 a plurality of second conductive lines along a
12 second direction on the dielectric layers and
13 the diodes, wherein the first direction is
14 perpendicular to the second direction.

1 2. The mask read only memory containing diodes as
2 claimed in claim 1, wherein the diodes are PN diodes.

1 3. The mask read only memory containing diodes as
2 claimed in claim 2, wherein the PN diodes comprise two
3 polysilicon layers of opposing conductive types.

1 4. The mask read only memory containing diodes as
2 claimed in claim 1, wherein the insulating layer is
3 silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride
4 (Si_3N_4), tantalum pentoxide (Ta_2O_5), barium strontium
5 titanate (BST), hafnium oxide (HfO_2), or titanium dioxide
6 (TiO_2).

1 5. The mask read only memory containing diodes as
2 claimed in claim 1, wherein the first conductive lines
3 are bit lines and the second conductive lines are word
4 lines.

1 6. The mask read only memory containing diodes as
2 claimed in claim 1, wherein the dielectric layers are
3 silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride
4 (Si_3N_4), tantalum pentoxide (Ta_2O_5), barium strontium
5 titanate (BST), hafnium oxide (HfO_2), or titanium dioxide
6 (TiO_2).

1 7. The mask read only memory containing diodes as
2 claimed in claim 1, comprising:

3 a semiconductor substrate;

4 an insulating layer on the semiconductor substrate;

5 and

6 at least two memory cell layers stacked on the
7 insulating layer wherein there is a separating
8 layer between any two memory cell layers to
9 provide insulation and wherein each memory cell
10 layer comprises:

11 a plurality of first conductive lines along a
12 first direction on the insulating layer;

13 a plurality of vertical diodes on the first
14 conductive lines;

15 a plurality of dielectric layers on part of the
16 diodes; and

17 a plurality of second conductive lines along a
18 second direction on the dielectric layers

19 and the diodes, wherein the first
20 direction is perpendicular to the second
21 direction,
22 wherein any two adjacent upper and lower diode
23 layers are disposed opposite to one
24 another so that two sides thereof of
25 opposing conductive type face each other.

1 8. The mask read only memory containing diodes as
2 claimed in claim 7, which comprises 2 to 10 memory cell
3 layers.

1 9. The mask read only memory containing diodes as
2 claimed in claim 7, wherein the separating layer is
3 silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride
4 (Si_3N_4), tantalum pentoxide (Ta_2O_5), barium strontium
5 titanate (BST), hafnium oxide (HfO_2), or titanium dioxide
6 (TiO_2).

1 10. The mask read only memory containing diodes as
2 claimed in claim 1, comprising:
3 a semiconductor substrate;
4 an insulating layer on the semiconductor substrate;
5 n diode layers stacked on the insulating layer,
6 wherein n is an integer equal to or greater
7 than 2 and each diode layer comprises a
8 plurality of vertical diodes and a plurality of
9 dielectric layers on part of the diodes; and
10 (n + 1) parallel conductive layers disposed between
11 the bottom diode layer and the insulating
12 layer, on the top diode layer, and between any

13 two adjacent diode layers respectively, wherein
14 the $(n + 1)$ parallel conductive layers are
15 disposed so that any two adjacent conductive
16 layers are perpendicular to each other,
17 wherein any two adjacent upper and lower diode
18 layers are disposed opposite to one another so
19 that two sides of matching conductive type face
20 each other.

1 11. The mask read only memory containing diodes as
2 claimed in claim 10, wherein n is between 2 and 10.

1 12. A method of manufacturing mask read only memory
2 containing diodes, comprising the steps of:

3 forming an insulating layer, a first conductive
4 layer, a second conductive layer and a third
5 conductive layer on a semiconductor substrate
6 in order, wherein a PN junction or Schottky
7 interface is formed between the second and the
8 third conductive layers;

9 patterning the third, the second, and the first
10 conductive layer, thereby forming a plurality
11 of first trenches along a first direction to
12 define the first conductive layer as a
13 plurality of bit lines;

14 filling a first insulating material into the first
15 trenches;

16 forming a dielectric layer on the entire surface of
17 the third conductive layer and the first
18 insulating material;

19 patterning the dielectric layer, the first
20 insulating material, the third conductive layer
21 and the second conductive layer and stopping
22 the patterning at the bit lines, thereby
23 forming a plurality of second trenches along a
24 second direction and forming a plurality of
25 diodes comprising the second conductive layer
26 and the third conductive layer, wherein the
27 first direction is perpendicular to the second
28 direction;

29 filling a second insulating material into the second
30 trenches so that the top of the second
31 insulating material is higher than that of the
32 dielectric layer, thereby forming a plurality
33 of third trenches along the second direction;

34 patterning the dielectric layer to expose part of
35 the third conductive layer of the diode,
36 thereby forming a plurality of openings for
37 coding defined as a plurality of codes; and
38 forming a fourth conductive layer on the entire
39 surface of the substrate and into the third
40 trenches and the openings for coding, thereby
41 forming a plurality of word lines.

1 13. The method as claimed in claim 12, wherein the
2 diodes are PN diodes.

1 14. The method as claimed in claim 13, wherein the
2 PN diode comprises two polysilicon layers of opposing
3 conductive types.

1 15. The method as claimed in claim 12, wherein the
2 dielectric layer is silicon dioxide, aluminum oxide (Al-
3 O_3), silicon nitride (Si_3N_4), tantalum pentoxide (Ta_2O_5),
4 barium strontium titanate (BST), hafnium oxide (HfO_2), or
5 titanium dioxide (TiO_2).

1 16. A method of manufacturing a mask read only
2 memory containing diodes, comprising the steps of:

3 forming an insulating layer, a first conductive
4 layer, a second conductive layer, a third
5 conductive layer, and a first dielectric layer
6 on a semiconductor substrate in order, wherein
7 a PN junction or Schottky interface is formed
8 between the second and the third conductive
9 layers;

10 patterning the first dielectric layer to expose part
11 of the third conductive layer, thereby forming
12 a plurality of first openings for coding
13 defined as a plurality of first codes;

14 patterning the first dielectric layer, the third
15 conductive layer, the second conductive layer
16 and the first conductive layer, thereby forming
17 a plurality of first trenches along a first
18 direction to define the first conductive layer
19 as a plurality of first bit lines;

20 filling a first insulating material into the first
21 trenches;

22 forming a fourth conductive layer on the surface of
23 the entire substrate and into the first
24 openings for coding;

forming a fifth conductive layer, a sixth conductive layer and a second dielectric layer on the fourth conductive layer in order, wherein a PN junction or Schottky interface between the fifth and the sixth conductive layers is formed;

patterning the second dielectric layer to expose part of the sixth conductive layer, thereby forming a plurality of second openings for coding defined as a plurality of second codes;

patterning the second dielectric layer, the sixth conductive layer, the fifth conductive layer, the fourth conductive layers, the first dielectric layer, the third conductive layer, and the second conductive layer, and stopping the patterning at the first bit lines, thereby forming a plurality of second trenches along a second direction to define the fourth conductive layer as a plurality of first word lines, wherein the first direction is perpendicular to the second direction;

filling a second insulating material into the second trenches;

forming a seventh conductive layer on the surface of the entire substrate and into the second openings for coding;

forming an eighth conductive layer, a ninth conductive layer and a third dielectric layer on the seventh conductive layer in order, wherein a PN junction or Schottky interface

55 between the eighth and the ninth conductive
56 layers is formed;
57 patterning the third dielectric layer to expose part
58 of the ninth conductive layer, thereby forming
59 a plurality of third openings for coding
60 defined as a plurality of third codes;
61 patterning the third dielectric layer, the ninth
62 conductive layer, the eighth conductive layer,
63 the seventh conductive layer, the second
64 dielectric layer, the sixth conductive layer
65 and the fifth conductive layer, and stopping
66 the patterning at the first word lines, thereby
67 forming a plurality of third trenches along the
68 first direction to define the seventh
69 conductive layer as a plurality of second bit
70 lines;
71 filling a third insulating material into the third
72 trenches;
73 patterning the third dielectric layer, the ninth
74 conductive layer and the eighth conductive
75 layer and stopping the patterning at the second
76 bit lines, thereby forming a plurality of
77 fourth trenches along the second direction;
78 filling a fourth insulating material into the fourth
79 trenches so that the top of the fourth
80 insulating material is higher than that of the
81 third dielectric layer, thereby forming a
82 plurality of the fifth trenches along the
83 second direction; and

84 filling a tenth conductive layer into the fifth
85 trenches, thereby forming a plurality of second
86 word lines,
87 wherein the third and the fifth conductive layers
88 are of matching conductive type and the sixth
89 and the eighth conductive layers are of
90 matching conductive type.

1 17. The method as claimed in claim 16, wherein the
2 second, the third, the fifth, the sixth, the eighth and
3 the ninth conductive layers are doped polysilicon layers.

1 18. The method as claimed in claim 17, wherein the
2 second, the sixth and the eighth conductive layers are of
3 matching conductive type and the third, the fifth and the
4 ninth conductive layers are of matching conductive type.

1 19. The method as claimed in claim 16, wherein the
2 first, the second, and the third dielectric layers are
3 silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride
4 (Si_3N_4), tantalum pentoxide (Ta_2O_5), barium strontium
5 titanate (BST), hafnium oxide (HfO_2), or titanium dioxide
6 (TiO_2).